



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Chi-Chun Chen et al.

Serial No. 10/600,393

Filed: June 20, 2003

For: Method of Forming Dual Gate Insulator
Layers for CMOS Applications

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Group Art Unit: 2812

Examiner: Thomas, Toniae M.

Conf. No.: 8529

INFORMATION DISCLOSURE STATEMENT

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The cited patents are listed in numerical order and are not in any order based on their pertinence.

Accompanying this transmittal is the \$180.00 fee set forth in 37 CFR §1.17(p) for submission of an Information Disclosure Statement under §1.97(c).

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account 08-1394.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

12/30/2004 HVUONG1 00000023 10600393

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180.00 DP

Respectfully submitted,

David M. O'Dell

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Date: 12-22-04

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R-94499.1

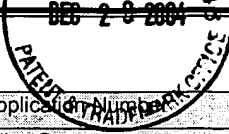

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Bonnie Boyle

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Signature

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	<div style="text-align: center;">  </div> <div style="text-align: right; font-size: small;">Complete if Known</div> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Application Number</td> <td>10/600,393</td> </tr> <tr> <td>Filing Date</td> <td>June 20, 2003</td> </tr> <tr> <td>Applicant(s)</td> <td>Chi-Chun Chen et al.</td> </tr> <tr> <td>Art Unit</td> <td>2822</td> </tr> <tr> <td>Examiner Name</td> <td>Thomas, Toniae M.</td> </tr> <tr> <td>Attorney Docket Number</td> <td>2002-0066 / 24061.461</td> </tr> </table> <div style="text-align: center;">  </div>	Application Number	10/600,393	Filing Date	June 20, 2003	Applicant(s)	Chi-Chun Chen et al.	Art Unit	2822	Examiner Name	Thomas, Toniae M.	Attorney Docket Number	2002-0066 / 24061.461
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>														
SHEET	1	OF 1												

U. S. PATENT DOCUMENTS				
Examiner's Initials	Cite No.	Document Number	Publication Date <small>MM-DD-YYYY</small>	Name of Patentee or Applicant of Cited Document
	AA	5960289	09-28-1999	Tsui et al.
	AB	6030862	02-29-2000	Kepler
	AC	6037224	03-14-2000	Buller et al.
	AD	6110842	08-29-2000	Okunno et al.
	AE	6121091	09-19-2000	Wang
	AF	6262455	07-17-2001	Lutze et al.
	AG	6294421	09-25-2001	Gonzalez et al.

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document <small>(Country Code - Number - Kind)</small>	Publication Date <small>MM-DD-YYYY</small>	Patentee or Applicant of Cited Document	Translation <small>Y/N</small>

OTHER PRIOR ART		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	AH	G. LUCOVSKY et al., "Formation of thin film dielectrics by remove plasma-enhanced chemical-vapor deposition (remote PECVD)", Applied Surface Science, Volume 39, Issue 1-4, October 1989, Pages 33-36.
	AI	STANLEY WOLF et al., "Silicon Processing For The VLSI Era, Volume 1: Process Technology", Lattice Press, Sunset Beach, CA, 3 pages
	AJ	HOWARD CHIH-HAO WANG et al., "Hot Carrier Reliability Improvement by Utilizing Phosphorus Transient Enhanced Diffusion for Input/Output Devices of Deep Submicron CMOS Technology", IEEE Electronic Device Letters, Vol. 21, No. 12, December 2000, 2 pages
	AK	HOWARD CHIH-HAO WANG et al., "Arsenic/Phosphorus LDD Optimization by Taking Advantage of Phosphorus Transient Enhanced Diffusion for High Voltage Input/Output CMOS Devices", IEEE Transactions on Electron Devices, Volume 49, No. 1, January 2002, 5 pages.